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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,793	BHATTACHARYYA, ARUP	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/16/07 and 01/29/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 01/16/07 has been entered.

Response to Arguments

2. Applicant's arguments with respect to the rejection(s) of claim(s) 33, 42, 54 and 63 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. A new ground(s) of rejection has made in view of the disclosure of an older reference.

Priority

3. Applicants have made no claim for priority.

Information Disclosure Statement

4. The Information Disclosure Statements filed on 01/16/07 and 01/29/07 have been considered.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over HORCH ET AL. (6,965,129) in view of READ, JR. (2,899,646).

In *Ex parte* CAROLYN RAMSEY CATAN, 83 USPQ2d 1569 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), an expanded panel of the Board of Appeals had the opportunity to discuss recent holdings, found in *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 82 USPQ2d 1385 (2007), concerning the obviousness of combinations such as the one Applicants claim. The panel began with the *Graham v. John Deere* analysis:

> The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). *See also KSR*, 127 S.Ct. at 1734, 82 USPQ2d at 1391 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.") The Court in *Graham* further noted that evidence of secondary considerations, such as commercial success, long felt but unsolved needs, failure of others, etc., "might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." 383 U.S. at 18, 148 USPQ at 467.

Ex parte Catan, 83 USPQ2d at 1572. The panel then explained,

> In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, 82 USPQ2d at 1395, and discussed circumstances in which a patent might be determined to be obvious without an explicit application of the teaching, suggestion, motivation test.
>
> In particular, the Supreme Court emphasized that "the principles laid down in *Graham* reaffirmed the 'functional approach' of *Hotchkiss*, 11 How. 248." *KSR*, 127 S.Ct. at 1739, 82 USPQ2d at 1395 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12, 148 USPQ 459, 464 (1966) (emphasis added)), and reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.*

Id. at 1573 The panel quoted *KSR* for the principles that

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id., quoting *KSR v. Teleflex,* 127 S.Ct. at 1740, 82 USPQ2d at 1396. The panel then explained, "The operative question in this 'functional approach' is thus 'whether the improvement is more than the predictable use of prior art elements according to their established functions'" *Id.* The panel cautioned that the question of whether the claimed invention is no more than a "predictable use of prior art elements according to their established functions" must be based on factual determinations requiring explicit findings on the Examiner's part. The panel stated, "[t]o facilitate review, [the Examiner's] analysis should be made explicit." *Id.* The panel went on to cite *In re Kahn* for the principle that "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*, quoting *In re Kahn,* 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

It is necessary, as the *CATAN* panel points out, to begin with the factual findings required by *Graham*. With regard to claims 1-5, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 having a floating node 339 or 939, the floating node 339 or 939 to store a charge indicative of a memory state of the memory cell; and a gate-controlled diode 330 or 930 exhibiting

Negative Differential Resistance (NDR) behavior connected between the floating node 339 or 939 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 including an anode 332 or 932 and a cathode 338 or 938, wherein the cathode 338 or 938 of the diode 330 or 930 may be connected to the floating node 339 or 939 of the access transistor 350 or 360 and the access transistor 350 or 360 may be formed in either a bulk semiconductor (note figures 3 and 9) structure or a semiconductor-on-insulator (note figures 1 and 2) structure. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. Nor is this Examiner required to prolong this already burdensome exercise by dwelling on matters that would have been in the common knowledge and common understanding of one of skill in the art. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *CATAN*, 83 USPQ2d at 1573, quoting *KSR*, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by

Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

As the *Graham* Court cautions, one may not ignore evidence of secondary considerations, especially "unexpected results." For evidence of unexpected results one must rely on Applicants. Applicants have actually made the claimed combination. Evidence of differences between results of the actual functioning of the claimed combination and the results of the functioning one of skill in the art would have had reason to predict (i.e., the "expected results") must necessarily come from one who has actually made the combination. A clear case of unexpected results would be if the claimed combination of prior art elements did not in fact perform according to their established functions in a predictable fashion; a result sometimes referred to as "synergy." See *Anderson's-Black Rock v. Pavement Co.* 396 U.S. 57, 61 (1969) (note that the *Anderson's-Black Rock* Court does not actually use the word, "synergy"). However, it is clear from the original *Graham* analysis (still good law, see *KSR v. Teleflex,* 127 S.Ct. at 1740, 82 USPQ2d at 1395) that any type of unexpected results (and indeed any type of secondary considerations) must be considered. Applicants' specification, however, does not include any evidence of secondary considerations. Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 6: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 having a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435, and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; a Negative Differential Resistance (NDR) diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 including an anode 332 or 932; a cathode 338 or 938; and a diode gate 913. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 7: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an n-channel access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the n-channel access transistor 350 or 360 having a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 330 or 930 having an n-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 in contact with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, col-

umn 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 8: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising a p-channel access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the p-channel access transistor 350 or 360 having a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 330 or 930 having an n-type anode 332 or

932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 9: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an n-channel access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the p-channel access transistor 350 or 360 having a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430

or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 330 or 930 having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 10: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising a p-channel access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the p-channel access transistor 350 or 360 having a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 330 or 930 having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 in contact with the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch

et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 11: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the access transistor 350 or 360 having a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being laterally oriented over the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative

resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 12: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 on a bulk semiconductor (note figures 3 and 9) substrate, the access transistor 350 or 360 having a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being vertically oriented over the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance di-

ode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 13: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an n-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the n-channel access transistor 350 or 360 having a floating body (part of second diffusion 2) and a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 330 or 930 having an n-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 in contact with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance

diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 14: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising a p-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the p-channel access transistor 350 or 360 having a floating body (part of second diffusion 2) and a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 330 or 930 having an n-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and a p-type cathode 338 or 938 in contact with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note,

column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 15: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an n-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the p-channel access transistor 350 or 360 having a floating body (part of second diffusion 2) and a n-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and an n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resis-

tance (NDR) p/n diode 330 or 930 having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 16: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising a p-channel access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the p-channel access transistor 350 or 360 having a floating body (part of second diffusion 2) and a p-type first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a p-type second diffusion region 354 (fig. 3) or 356 (fig. 9), the p-type second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 330 or 930 having a p-type anode 332 or 932 connected to a diode reference potential line 440 (see fig. 4) and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in

said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 17: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the access transistor 350 or 360 having a floating body (part of second diffusion 2) and a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and an n-type cathode 338 or 938 formed with the n-type second diffusion region 354 (fig. 3) or 356 (fig. 9), said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode

used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 18: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the access transistor 350 or 360 having a floating body (part of second diffusion 2) and a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being vertically oriented over the access transistor 350 or 360, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 19: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 on a semiconductor-on-insulator (note figures 1 and 2) substrate, the access transistor 350 or 360 having a floating body (part of second diffusion 2) and a first diffusion region 356 (fig. 3) or 364 (fig. 9) connected to a bit line 430 or 435 and a second diffusion region 354 (fig. 3) or 356 (fig. 9), the second diffusion region 354 (fig. 3) or 356 (fig. 9) to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 and a diode reference potential line 440 (see fig. 4), the diode 330 or 930 having an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being vertically oriented over the access transistor 350 or 360, said cell being reasonable capable, should circumstances arise, of performing the function of

enhancing diode 330 or 930 switching with intentionally-generated charges in the floating body of the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 20-28, 30, and 31: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360, including a body region 355 or 365; a first diffusion region 356 (fig. 3) or 364 (fig. 9) electrically connected to a bit line 430 or 435; a second diffusion region 354 (fig. 3) or 356 (fig. 9)

separated from the first diffusion region 356 (fig. 3) or 364 (fig. 9) by a channel area in the body region 355 or 365; a gate (seen attached to word line 424 or 484) separated from the channel area by a gate insulator (seen between the gate and body region 355 or 365), the gate electrically connected to a word line 424 or 484; a Negative Differential Resistance (NDR) diode 330 or 930, including an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode reference potential line 440 (see fig. 4), said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 354 (fig. 3) or 356 (fig. 9) that may be representative of a memory state, wherein the access transistor 350 or 360 may include an n-channel transistor or a p-channel transistor, wherein the diode 330 or 930 may include a p/n diode 330 or 930 having a p-type anode 332 or 932 and an n-type cathode 338 or 938, the p/n diode 330 or 930 may include a p+/n+ diode 330 or 930 having a p+ anode 332 or 932 and an n+ cathode 338 or 938, the diode 330 or 930 may include an n/p diode 330 or 930 having an n-type anode 332 or 932 and a p-type cathode 338 or 938, or an n+/p diode 330 or 930 having an n+ anode 332 or 932 and a p cathode 338 or 938, wherein the diode 330 or 930 may include a laterally-oriented or vertically-oriented diode 330 or 930 or a gate-controlled diode 330 or 930 to enhance switching performance and reduce standby power, and the access transistor 350 or 360 may be on a semiconductor-on-insulator (note figures 1 and 2) or bulk semiconductor (note figures 3 and 9) substrate. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would

have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 29: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360, including a body region 355 or 365; a first diffusion region 356 (fig. 3) or 364 (fig. 9) electrically connected to a bit line 430 or 435; a second diffusion region 354 (fig. 3) or 356 (fig. 9) separated from the first diffusion region 356 (fig. 3) or 364 (fig. 9) by a channel area in the body region 355 or 365; a gate (seen attached to word line 424 or 484) separated from the channel area by a gate insulator (seen between the gate and body region 355 or 365), the gate electrically connected to a word line 424 or 484; a Negative Differential Resistance (NDR) diode 330 or 930, including an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode reference potential line 440 (see fig. 4), said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 354 (fig. 3) or 356 (fig. 9) that may be representative of a memory state. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose that the diode is formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabi-

lizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14, having a desired geometry to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 33-41: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360 formed in a bulk semiconductor (note figures 3 and 9) structure, the access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region 356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a gate-controlled Negative Differential Resistance (NDR) diode 330 or 930 connected between a reference potential line 440 (see fig. 4) and the second diffusion region 354 (fig. 3) or 356 (fig. 9), the diode 330 or 930 including an anode 332 or 932, a cathode 338 or 938, and a diode gate 313 or 913 connected to a second word line 420 or 480, wherein the gate-controlled diode 330 or 930 may in-

clude a laterally-oriented diode 330 or 930 positioned over the access transistor 350 or 360, or a vertically-oriented diode 330 or 930, the first and second diffusion region 354 (fig. 3) or 356 (fig. 9)s of the access transistor 350 or 360 include n-type or p-type dopants; and the gate-controlled diode 330 or 930 may include a p/n or n/p diode 330 or 930 having a p-type or n-type anode 332 or 932 connected to the reference potential line 440 (see fig. 4) and an n-type or p-type cathode 338 or 938 formed with the second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or side-ways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

The applicant's claim 36 does not distinguish over the Horch et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a "product by process" claim can be anticipated by a reference that does not recite said process. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1100. The Federal Circuit cited with approval this Office's current statement of the law, found in MPEP § 2113:

> [Even] though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) ("Although in some instances a claim may validly describe a new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced."). Id.

Horch et al. does not disclose that the diode is formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and be operatively positioned to enhance switching performance. However, Read, Jr. discloses a P-I-N negative resistance diode 10 formed so as to include an intrinsic region 13, between an anode 11 and a cathode 14 of the diode, having a desired geometry to assist with stabilizing the state of the diode and be operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 42-53: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an semiconductor-on-insulator (note figures 1 and 2) (SOI) structure, including an SOI access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region 356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a Negative Differential Resistance (NDR) diode 330 or 930 connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a reference potential line 440 (see fig. 4), the diode 330 or 930 including an anode 332 or 932, a cathode 338 or 938, a diode gate 313 or 913 connected to a second word line 420 or 480; the anode 332 or 932 and the cathode 338 or 938 having a desired geometry to store a charge indicative of a memory state and being operably positioned with respect to the diode gate 313 or 913, wherein the diode 330 or 930 may include a lateral-oriented diode 330 or 930 positioned over the access transistor 350 or 360 and the SOI access transistor 350 or 360 and the lateral-oriented diode 330 or 930 may be formed in a semiconductor volume over a buried oxide (BOX) region, the diode 330 or 930 may include a vertical-oriented diode 330 or 930 including the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360, and the first and second diffusion region 354 (fig. 3) or 356 (fig. 9)s of the access transistor 350 or 360 may include n-type or p-type dopants; and the gate-controlled diode 330 or 930 may include a p/n or n/p diode 330 or 930 having an n-type or p-type anode 332 or 932 connected to the reference potential line 440 (see fig. 4) and a p-type or n-type cathode 338 or 938 formed with the second diffusion region 354 (fig. 3) or 356 (fig. 9). Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. *CATAN*, 83 USPQ2d at 1573, quoting *KSR*, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

The applicant's claim 46 does not distinguish over the Horch et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Horch et al. does not disclose an intrinsic region between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 54-62: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360, the access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region

356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a Negative Differential Resistance (NDR) p+/n+ diode 330 or 930 connected between a diode reference potential line 440 (see fig. 4) and the second diffusion region 354 (fig. 3) or 356 (fig. 9), the p/n diode 330 or 930 including a p+ anode 332 or 932, an n+ cathode 338 or 938, and a diode gate 313 or 913 connected to a second word line 420 or 480, wherein the diode 330 or 930 may include a laterally-oriented or vertically-oriented diode 330 or 930 or a gate-controlled diode 330 or 930 to enhance switching performance and reduce standby power, and the access transistor 350 or 360 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figures 1 and 2) or bulk semiconductor (note figures 3 and 9) substrate. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. Horch et al. does not disclose an intrinsic region operably positioned between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 63-71: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory cell, comprising an access transistor 350 or 360, the access transistor 350 or 360 including a first diffusion region 356 (fig. 3) or 364 (fig. 9) separated from a second diffusion region 354 (fig. 3) or 356 (fig. 9) by a channel region, and further including a gate (seen attached to word line 424 or 484) separated from the channel region by a gate insulator (seen between the gate and body region 355 or 365), wherein the first diffusion region 356 (fig. 3) or 364 (fig. 9) may be connected to a bit line 430 or 435 and the gate may be connected to a first word line 424 or 484; and a Negative Differential Resistance (NDR) n+/p diode 330 or 930 connected between a diode reference potential line 440 (see fig. 4) and the second diffusion region 354 (fig. 3) or 356 (fig. 9), the p/n diode 330 or 930 including an n+ anode 332 or 932, a p cathode 338 or 938, and a diode gate 313 or 913 connected to a second word line 420 or 480, wherein the diode 330 or 930 may include a laterally-oriented or vertically-oriented diode 330 or 930 or a gate-controlled diode 330 or 930 to enhance switching performance and reduce standby power, and the access transistor 350 or 360 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figures 1 and 2) or bulk semiconductor (note figures 3 and 9) substrate. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Horch et al. does not disclose an intrinsic region operably positioned between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance

diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 72-79: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Horch et al. teaches a memory device, comprising a memory array, including a plurality of memory cells in rows and columns; a number of word lines 424 and 484, each word line 424 or 484 connected to a row of memory cells; a number of bit lines 430 and 435, each bit line 430 or 435 connected to a column of memory cells; at least one reference line 440 to provide a reference potential to the memory cells; control circuitry, including word line 424 or 484, select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations, wherein each memory cell may include an access transistor 350 or 360, including a body region 355 or 365, a first diffusion region 356 (fig. 3) or 364 (fig. 9) electrically connected to one of the bit lines 430 and 435, a second diffusion region 354 (fig. 3) or 356 (fig. 9) separated from the first diffusion region 356 (fig. 3) or 364 (fig. 9) by a channel area in the body region 355 or 365, and a gate (seen attached to word line 424 or 484) separated from the channel area by a gate insulator (seen between the gate and body region 355 or 365) and electrically connected to one of the word lines 424 and 484; and a Negative Differential Resistance (NDR) gate-controlled diode 330 or 930, including an anode 332 or 932 and a cathode 338 or 938, the diode 330 or 930 being connected between the second diffusion region 354 (fig. 3) or 356 (fig. 9) and a diode 330 or 930 reference line, wherein the memory cell may be adapted to store a charge in the second diffusion region 354 (fig. 3) or 356 (fig. 9) of the access transistor 350 or 360 to indicate a stable memory state, wherein each memory cell may be on a bulk semiconductor (note figures 3 and 9) substrate, and the diode 330 or 930 may include a vertically-oriented diode 330 or 930 or a laterally-oriented diode 330 or 930 over

the access transistor 350 or 360, or each memory cell may be on a semiconductor-on-insulator (note figures 1 and 2) substrate such that the access transistor 350 or 360 has a floating body (part of second diffusion 2), and the diode 330 or 930 may include a laterally-oriented diode 330 or 930 formed over, or at least partially in the floating body of, the access transistor 350 or 360. Note figures 1-4,9, column 6 lines 42-67, column 7, column 8 lines 31-67, and column 10 lines 39-67 of Horch et al. Note, column 11 lines 41-57, that Horch et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. *CATAN*, 83 USPQ2d at 1573, quoting *KSR*, 127 S.Ct. at 1741, 82 USPQ2d at 1396.

Horch et al. does not disclose an intrinsic region between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. conclusively proves, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Horch et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Horch et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Horch et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Horch et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Horch et al.'s memory cell, and that in said combination Horch et al.'s memory cell would continue functioning in the manner disclosed by Horch et al. It would therefore have been obvious to a person having skill in the art to modify Horch et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Horch et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

B. Applicants will be aware that, date-wise, Horch et al. does not present an insurmountable bar to the patentability of their claims. In the interests of compact prosecution, therefore, claims 1-79 are

rejected under 35 U.S.C. 103(a) as being unpatentable over NEMATI ET AL. (6,229,161) (published 5/8/2001) in view of READ, JR. (2,899,646).

Again, in keeping with the guidance of *Ex parte* CAROLYN RAMSEY CATAN, 83 USPQ2d 1569 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL), we begin with the factual findings required by *Graham*. With regard to claims 1-5, Nemati et al. teaches a memory cell, comprising an access transistor 12 having a floating node 24, the floating node 24 to store a charge indicative of a memory state of the memory cell; and a gate-controlled diode 10 exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node 24 and a diode reference potential line 19, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), wherein the cathode of the diode 10 may be connected to the floating node 24 of the access transistor 12 and the access transistor 12 may be formed in either a bulk semiconductor (note figure 6) structure or a semiconductor-on-insulator (note figure 6a) structure. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." Nemati et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of

skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

As the *Graham* Court cautions, one may not ignore evidence of secondary considerations, especially "unexpected results." For evidence of unexpected results one must rely on Applicants. Applicants have actually made the claimed combination. Evidence of differences between results of the actual functioning of the claimed combination and the results of the functioning one of skill in the art would have had reason to predict (i.e., the "expected results") must necessarily come from one who has actually made the combination. A clear case of unexpected results would be if the claimed combination of prior art elements did not in fact perform according to their established functions in a predictable fashion; a result sometimes referred to as "synergy." See *Anderson's-Black Rock v. Pavement Co.* 396 U.S. 57, 61 (1969) (note that the *Anderson's-Black Rock* Court does not actually use the word, "synergy"). However, it is clear from the original *Graham* analysis (still good law, see *KSR v. Teleflex,* 127 S.Ct. at 1740, 82 USPQ2d at 1395) that any type of unexpected results (and indeed any type of secondary considerations) must be considered. Applicants' specification, however, does not include any evidence of secondary considerations. Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 6: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18, and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 and a diode reference potential line 19, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19); a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24); and a diode gate 20. Note figures 1-3, 6-8, column 4 lines 1-67, column 5

lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ."

Nemati et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode, and operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 7: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an n-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate, the n-channel access transistor 12 having a

n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the n-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nemati et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 8: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising a p-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate, the p-channel access transistor 12 having a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nemati et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s mem-

ory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 9: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an n-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate, the p-channel access transistor 12 having a n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nemati et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitut-

able for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 10: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising a p-channel access transistor 12 on a bulk semiconductor (note figure 6) substrate; the p-channel access transistor 12 having a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the p-type second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nemati et al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance di-

ode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 11: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12 on a bulk semiconductor (note figure 6) substrate, the access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being laterally oriented over the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance

diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 12: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12 on a bulk semiconductor (note figure 6) substrate, the access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being vertically oriented over the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-

side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 13: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an n-channel access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the n-channel access transistor 12 having a floating body (part of second diffusion 24) and a n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the unnumbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of

diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 14: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising a p-channel access transistor

12 on a semiconductor-on-insulator (note figure 6a) substrate, the p-channel access transistor 12 having a floating body (part of second diffusion 24) and a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and a p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) in contact with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the

manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 15: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an n-channel access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the p-channel access transistor 12 having a floating body (part of second diffusion 24) and a n-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and an n-type second diffusion region 24, the n-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance di-

ode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 16: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising a p-channel access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the p-channel access transistor 12 having a floating body (part of second diffusion 24) and a p-type first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a p-type second diffusion region 24, the p-type second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to a diode reference potential line 19 and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance

diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 17: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the access transistor 12 having a floating body (part of second diffusion 24) and a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the n-type second diffusion region 24, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4

lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 18: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the access transistor 12 having a floating body (part of second diffusion 24) and a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resis-

tance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being vertically oriented over the access transistor 12, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 19: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12 on a semiconductor-on-insulator (note figure 6a) substrate, the access transistor 12 having a floating body (part of second diffusion 24) and a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second diffusion region 24, the second diffusion region 24 to store a charge indicative of a memory state of the memory cell; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 of the access transistor 12 and a diode reference potential line 19, the diode 10 having an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being vertically oriented over the access transistor 12, said cell being reasonable capable, should circumstances arise, of performing the function of enhancing diode 10 switching with intentionally-generated charges in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14 to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art

would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 20-28, 30, and 31: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12, including a body region 16; a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to a bit line 18; a second diffusion region 24 separated from the first diffusion region by a channel area in the body region 16; a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate 14), the gate 14 electrically connected to a word line 14 ; a Negative Differential Resistance (NDR) diode 10, including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being connected between the second diffusion region 24 and a diode reference potential line 19, said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 24 that may be representative of a memory state, wherein the access transistor 12 may include an n-channel transistor or a p-channel transistor, wherein the diode 10 may include a p/n diode 10 having a p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and an n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the p/n diode 10 may include a p+/n+ diode 10 having a p+ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and an n+ cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 may include an n/p diode 10 having an n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a p-type cathode (part of diode 10 that is adjacent to and

sometimes contiguous with node 24), or an n+/p diode 10 having an n+ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a p cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), wherein the diode 10 may include a laterally-oriented or vertically-oriented diode 10 or a gate-controlled diode 10 to enhance switching performance and reduce standby power, and the access transistor 12 may be on a semiconductor-on-insulator (note figure 6a) or bulk semiconductor (note figure 6) substrate.Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claim 29: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12, including a body region 16; a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to a bit line 18; a second diffusion region 24 separated from the first diffusion region by a channel area in the body region 16; a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate 14), the gate 14 electrically connected to a word line 14 ; a Negative Differential Resistance (NDR) diode 10, including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being connected between the second diffusion region 24 and a diode reference potential line 19, said cell being reasonable capable, should circumstances arise, of performing the function of operating to store and sense a charge in the second diffusion region 24 that may be representative of a memory state. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose that the diode is formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14, having a desired geometry to assist with stabilizing the state of the NDR diode. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resis-

tance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 33-41: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12 formed in a bulk semiconductor (note figure 6) structure, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14; and a gate-controlled Negative Differential Resistance (NDR) diode 10 connected between a reference potential line 19 and the second diffusion region 24, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), and a diode gate connected to a second word line 20, wherein the gate-controlled diode 10 may include a laterally-oriented diode 10 positioned over the access transistor 12, or a vertically-oriented diode 10, the first and second diffusion regions of the access transistor 12 include n-type or p-type dopants; and the gate-controlled diode 10 may include a p/n or n/p diode 10 having a p-type or n-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to the reference potential line 19 and an n-type or p-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject mat-

ter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ."

The applicant's claim 36 does not distinguish over the Nemati et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Nemati et al. does not disclose that the diode is formed so as to include an intrinsic region, between the anode and the cathode of the NDR diode, having a desired geometry to assist with stabilizing the state of the NDR diode and be operatively positioned to enhance switching performance. However, Read, Jr. discloses a P-I-N negative resistance diode 10 formed so as to include an intrinsic region 13, between an anode 11 and a cathode 14 of the diode, having a desired geometry to assist with stabilizing the state of the diode and be operatively positioned to enhance switching performance. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 42-53: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an semiconductor-on-insulator (note figure 6a) (SOI) structure, including an SOI access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14 ; and a Negative Differential Resistance (NDR) diode 10 connected between the second diffusion region 24 and a reference potential line 19, the diode 10 including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), a diode gate connected to a second word line 20; the anode and the cathode having a desired geometry to store a charge indicative of a memory state and being operably positioned with respect to the diode gate 20, wherein the diode 10 may include a lateral-oriented diode 10 positioned over the access transistor 12 and the SOI access transistor 12 and the lateral-oriented diode 10 may be formed in a semiconductor volume over a buried oxide (BOX) region, the diode 10 may include a vertical-oriented diode 10 including the second diffusion region 24 of the access transistor 12, and the first and second diffusion regions of the access transistor 12 may include n-type or p-type dopants; and the gate-controlled diode 10 may include a p/n or n/p diode 10 having an n-type or p-type anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) connected to the reference potential line 19 and a p-type or n-type cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24) formed with the second diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ."

The applicant's claim 46 does not distinguish over the Nemati et al. reference regardless of the process used to form the lateral-orientated diode, because only the final product is relevant, not the

recited process of using raised source/drain techniques and metal-induced-lateral crystallization techniques. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Nemati et al. does not disclose an intrinsic region between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 54-62: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14 ; and a Negative Differential Resistance (NDR) p+/n+ diode 10 connected between a diode reference potential line 19 and the second diffusion region 24, the p/n diode 10 including a

p+ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), an n+ cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), and a diode gate connected to a second word line 20, wherein the diode 10 may include a laterally-oriented or vertically-oriented diode 10 or a gate-controlled diode 10 to enhance switching performance and reduce standby power, and the access transistor 12 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figure 6a) or bulk semiconductor (note figure 6) substrate. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region operably positioned between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 63-71: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory cell, comprising an access transistor 12, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region may be connected to a bit line 18 and the gate 14 may be connected to a first word line 14 ; and a Negative Differential Resistance (NDR) n+/p diode 10 connected between a diode reference potential line 19 and the second diffusion region 24, the p/n diode 10 including an n+ anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19), a p cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), and a diode gate connected to a second word line 20, wherein the diode 10 may include a laterally-oriented or vertically-oriented diode 10 or a gate-controlled diode 10 to enhance switching performance and reduce standby power, and the access transistor 12 may include a p-channel or n-channel transistor on a semiconductor-on-insulator (note figure 6a) or bulk semiconductor (note figure 6) substrate. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings.

Nematiet al. does not disclose an intrinsic region operably positioned between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 operably positioned between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resis-

tance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

With regard to claims 72-79: Beginning (as suggested by the CATAN panel) with the factual findings required by Graham, Nemati et al. teaches a memory device, comprising a memory array, including a plurality of memory cells in rows and columns; a number of word lines 14, each word line 14 connected to a row of memory cells; a number of bit lines 12, each bit line 18 connected to a column of memory cells; at least one reference line 19 to provide a reference potential to the memory cells; control circuitry, including word line 14, select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations, wherein each memory cell may include an access transistor 12, including a body region 16, a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to one of the bit lines 12, a second diffusion region 24 separated from the first diffusion region by a channel area in the body region 16, and a gate separated from the channel area by a gate insulator (not numbered; seen under gate 14) and electrically connected to one of the word lines 14; and a Negative Differential Resistance (NDR) gate-controlled diode 10, including an anode (the un-numbered doped region [shown, for example, as a P region in figure 1] in diode 10 that is adjacent to reference line 19) and a cathode (part of diode 10 that is adjacent to and sometimes contiguous with node 24), the diode 10 being connected between the second diffusion region 24 and a diode reference line 19, wherein the memory cell may be adapted to store a charge in the second diffusion region 24 of the access transistor 12 to indicate a stable memory state, wherein each memory cell may be on a bulk semiconductor (note figure 6) substrate, and the diode 10 may include a vertically-oriented diode 10 or a laterally-oriented diode 10 over the access transistor 12, or each memory cell may be on a semiconductor-on-insulator (note figure 6a)

substrate such that the access transistor 12 has a floating body (formed from second diffusion 24), and the diode 10 may include a laterally-oriented diode 10 formed over, or at least partially in the floating body of, the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al. Note, column 7 lines 16-31, that Nemati et al. did not feel the need to explicitly describe variations (such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, or turning the diode N- or P-side down, or sideways) that they reasonably believed (as would any objective observer) would have been suggested to one of skill in the art by the explicit teachings. "[T]he analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." Nemati et al. does not disclose an intrinsic region between the anode and the cathode. However, Read, Jr. discloses a P-I-N negative resistance diode 10 with an intrinsic region 13 between an anode 11 and a cathode 14. Note figures 1-3, column 2 lines 3-49, and column 4 lines 12-54 of Read, Jr. Further, the disclosure of Read, Jr. proves conclusively, note column 1 lines 15-41, that those of skill in the art would have been familiar with a method of substituting a P-I-N negative resistance diode for Shockley 2,794,917's P-N negative resistance diode (the same negative resistance diode used in Nemati et al.'s memory cell). From the similarities between the P-I-N negative resistance diode and the P-N negative resistance diode of Nemati et al.'s memory cell, one of skill in the art would have been able to conclude that P-I-N negative resistance diode would have been substitutable for the P-N negative resistance diode of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on the similarity of its functioning to the functioning of the P-N negative resistance diode of Nemati et al.'s memory cell) that P-I-N negative resistance diode would have continued functioning much as it did before being substituted into Nemati et al.'s memory cell, and that in said combination Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the P-I-N negative resistance diode taught by Read, Jr. for the P-N negative resistance diode of Nemati et al.'s memory cell.

Note that Applicants disclose that the claimed combination "may be" made; Applicants do not disclose any unexpected results or indeed any results at all.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826